

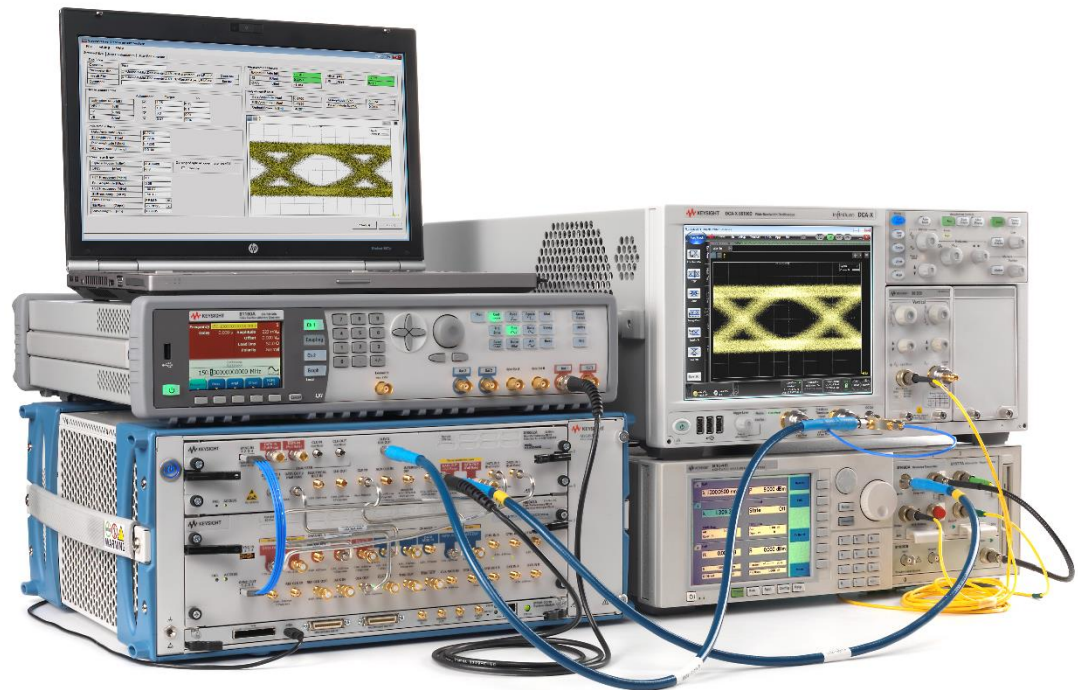
100/400G Ethernet Design – Advanced Characterization and Debug Solution – Part I

서동현

30/08/2016

N4917B

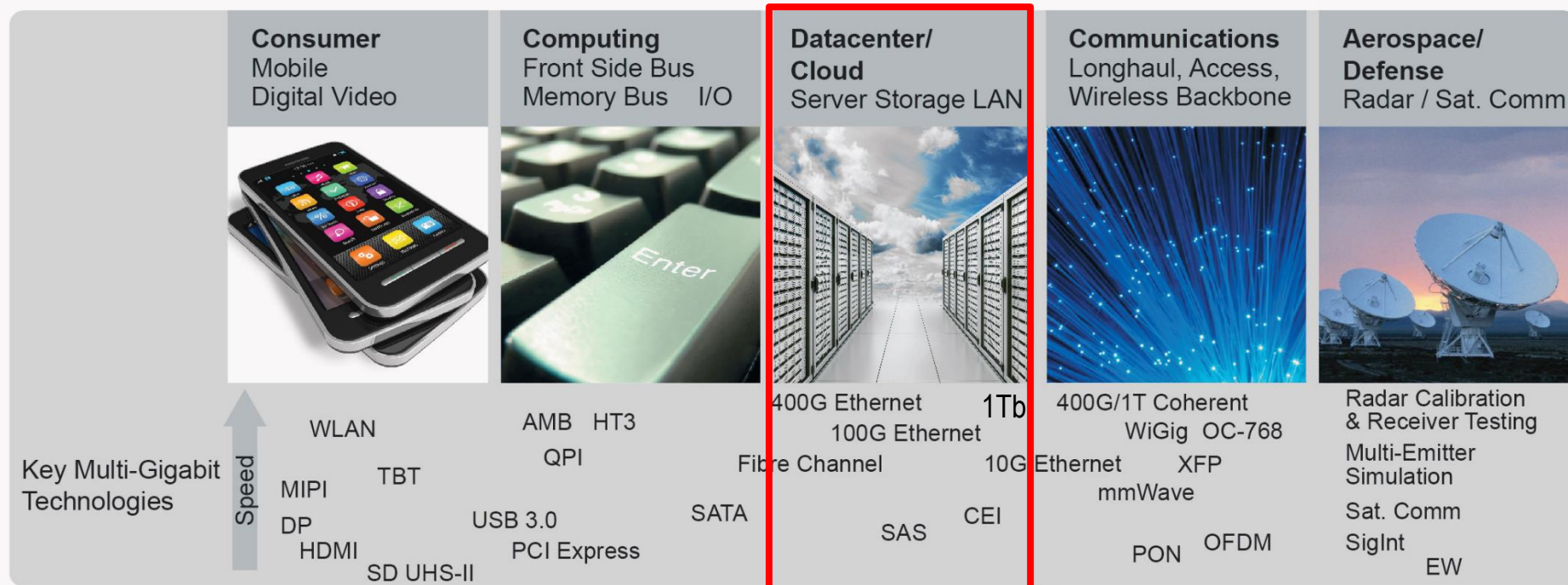
Optical Receiver Stress Test Solution



Agenda

- Market Overview, Segments, Customers
 - Application Requirements
 - Product Details
 - Configuration

Target High-Speed Digital Applications

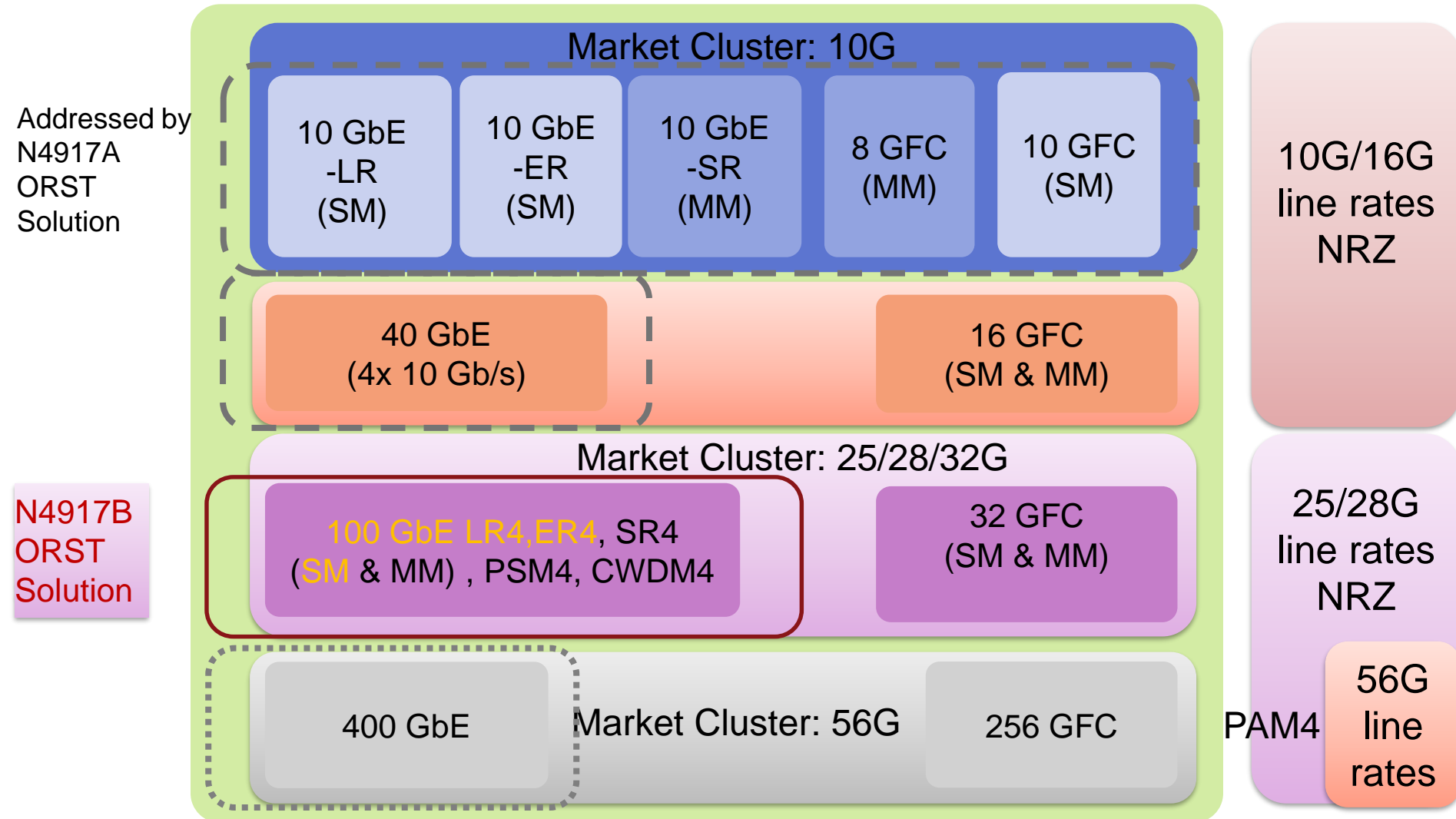


Cloud computing drives datacenter build-out

- Network bandwidth deploys 100GbE and 400GbE electrical on-board and optical off-board

Market Segments According to Standards

Parent market: data center



Application in Data Center ex Line Card



Main installation so far:

100GBASE LR4/ER4

- SP transport
- Routing (Router to WDM, RtoR)

Usage in true data center very limited so far

- Rack internal typically MM SR
- Top of rack aggregation layer typically MM or SM depending on distance
- Inter data center SM LR/ER type standards
- Edge router to external internet coherent for metro LR or LH

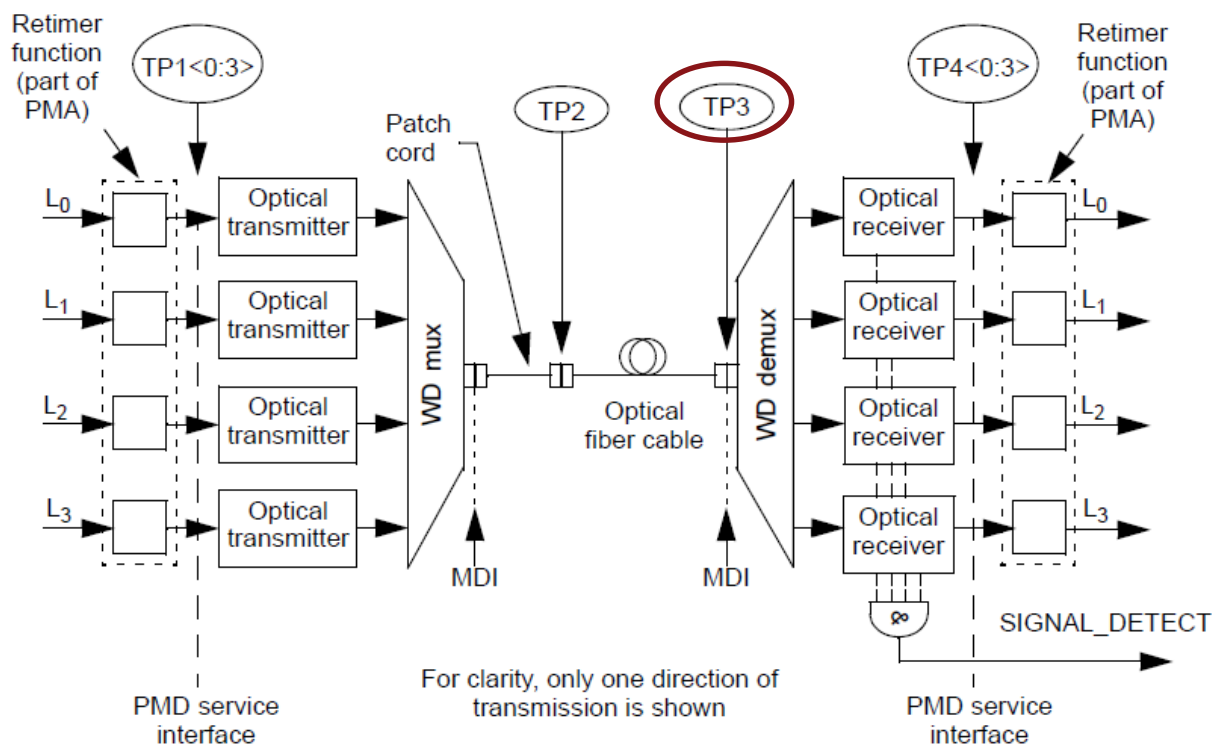


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Architecture of the 100GBASE-LR4/-ER4 TX/RX Path

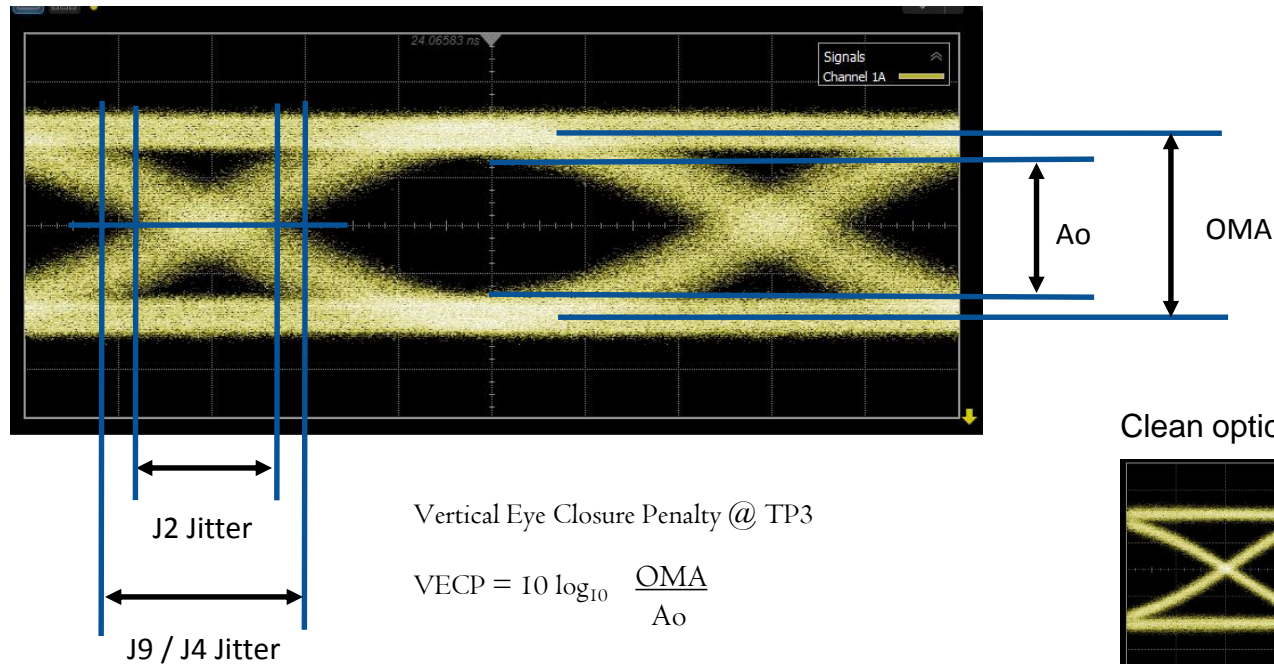
Only one direction shown



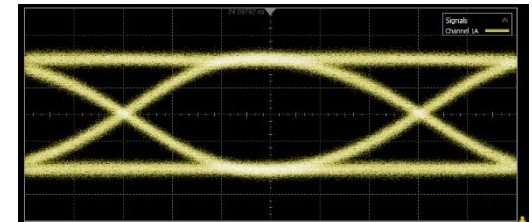
Source: IEEE 802.3-2015, Clause 88.5, Figure 88-2

What is “Optical Receiver Stress Test”

Parameters of stressed optical eye at TP3



Clean optical eye



Glossary:

- OMA:** Optical Modulation Amplitude, measured in [mW] (difference between one level and zero level)
ER: Extinction Ratio, measured in [dB] (ratio of one level to zero level)
VECP: Vertical Eye Closure Penalty, $10 \times \log OMA/A_o$, measured in [dB] (A_o is innermost eye opening with ISI)
UI: Unit Interval (one bit period)
J2,J4,J9: Time interval that includes 1-10⁻² (-4) (-9) of the total Jitter components.

IEEE 802.3 clause 88 requirements (-LR4/-ER4)

Clause 88 refers to clause 87 (40GBASE-LR4/-ER4)

- Receiver sensitivity is **informative**
Receiver sensitivity, which is defined for an ideal input signal, ...
- Stressed receiver sensitivity is **normative !**

Description	100GBASE-LR4	100GBASE-ER4	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm		GBd
Average receive power, each lane (max)	4.5		dBm
Average receive power, each lane (min)	-10.6	-20.9	dBm
Receive power, each lane (OMA) (max)	4.5		dBm
Receiver sensitivity (OMA), each lane (max)	-8.6	-21.4	dBm
Stressed receiver sensitivity (OMA), each lane ^f (max)	-6.8	-17.9	dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty ^f each lane	1.8	3.5	dB
Stressed eye J2 Jitter ^f each lane	0.30		UI
Stressed eye J9 Jitter ^f each lane	0.47		UI

Source: IEEE 802.3-2015, Clause 88.8, Table 88-8

J2/J9 and VECP Definition

$$\text{Vertical eye closure penalty} = 10\log_{10} \frac{OMA}{A_O} \quad (\text{dB}) \quad (87-1)$$

where

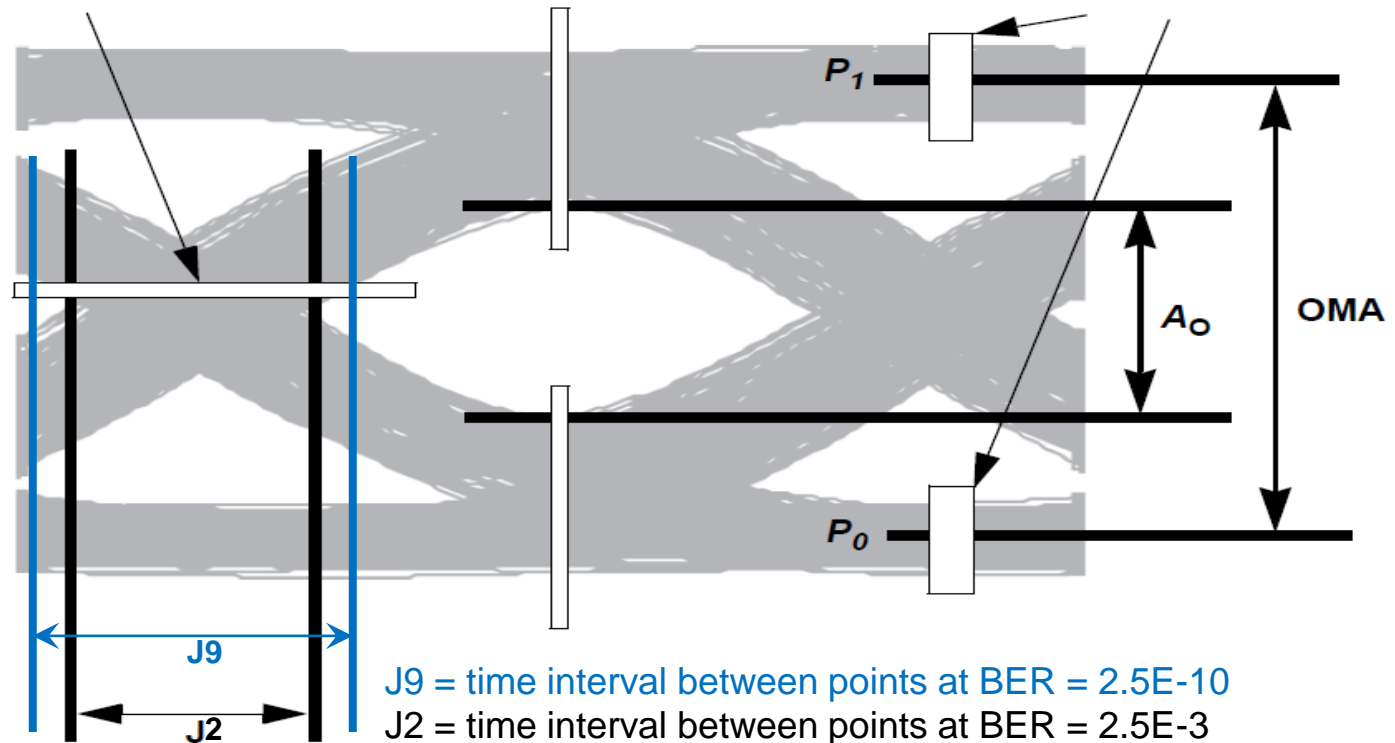
A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram

OMA is the optical modulation amplitude as defined in 87.8.5

Jitter histogram (at waveform average, may not be at waist)

Vertical eye closure histograms (at time-center of eye)

Approximate OMA (difference of means of histograms)



100GBASE-LR4/-ER4 and it's MSA's

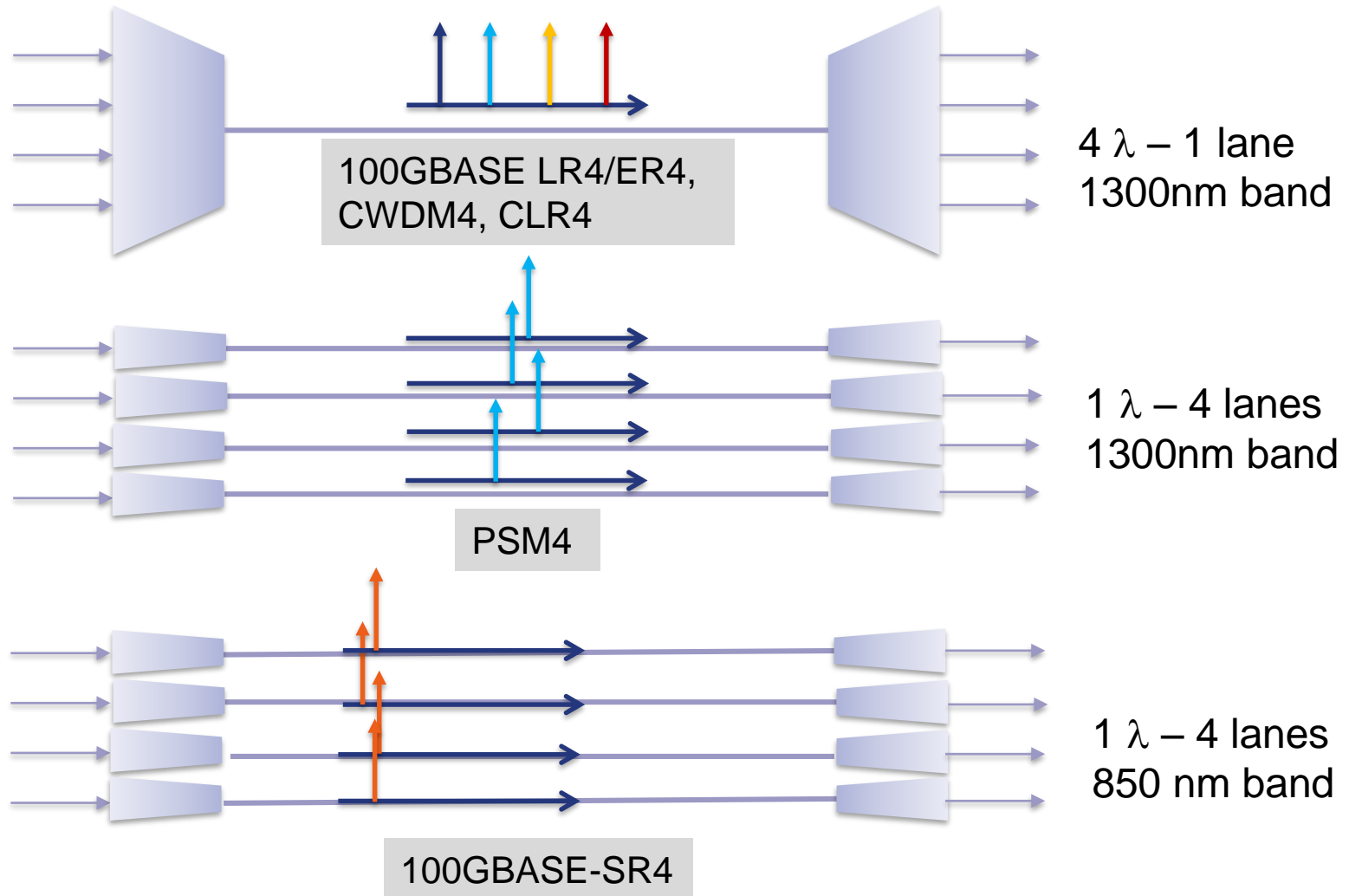
Variants refering to IEEE 802.3 clause 88 with modifications

Parameter	100GBASE-LR4	100GBASE-ER4	CLR4 w/o FEC	CLR4 w/ FEC	CWDM4 w/ FEC	PSM4 w/ FEC
Reach	2 m – 10 km	2 m – 40 km	2 m – 2 km	2 m – 2 km	2 m – 2 km	2m – 0.5 km
Stressed receiver sensitivity, OMA	-6.8 dBm	-17.9 dBm	-5.6 dBm	-8.5 dBm	-7.3 dBm	-8.8 dBm
BER target	1E-12	1E-12	1E-12	2.1E-5	5E-5	5E-5
Receiver vertical eye closure penalty (min)	1.8 dB	3.5 dB	1.95 dB	1.95 dB	1.9 dB	1.9 dB
Stressed eye J2 Jitter	0.3 UI	0.3 UI	0.3 UI	0.33 UI	0.33 UI	0.27 UI
Stressed eye J4 Jitter	-	-	-	0.48 UI	0.48 UI	0.39 UI
Stressed eye J9 Jitter	0.47 UI	0.47 UI	0.5 UI	-	-	-
Stessed eye mask Definiton (X1, X2, X3, Y1, Y2, Y3)	-	-	-	-	0.39,0.5,0.5, 0.39,0.39,0.4	0.24,0.5,0.5, 0.24,0.24,0.4
Used wavelength	4.5nm spacing 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19 (nm)	4.5nm spacing 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19 (nm)	20 nm spacing 1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5 (nm)	20 nm spacing 1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5 (nm)	20 nm spacing 1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5 (nm)	4 x 1295 to 1325 nm

No guarantee for correctness of parameters, standards may evolve!

Optical Differences Between PSM4, LR4, SR4

Only one direction is shown



IEEE 802.3 Clause 87/88 Stressed RX Test Setup

Generation of electrical stressed test signal

Pattern Generator:

Generates the **test pattern**

Frequency synthesizer:

Creates sinusoidally jittered clock, **periodic jitter (PJ)**

Sinusoidal Amplitude Interferer 1:

Causes bit shrinkage (DDPWS) in conjunction with limiter

Gaussian Noise Generator:

Causes **random jitter (RJ)** in conjunction with limiter

Sinusoidal Amplitude Interferer 2:

Causes additional **vertical eye-closure (VECP)** and sinusoidal jitter (SJ)

Low-pass filter:

Creates ISI-induced vertical eye closure (VECP)

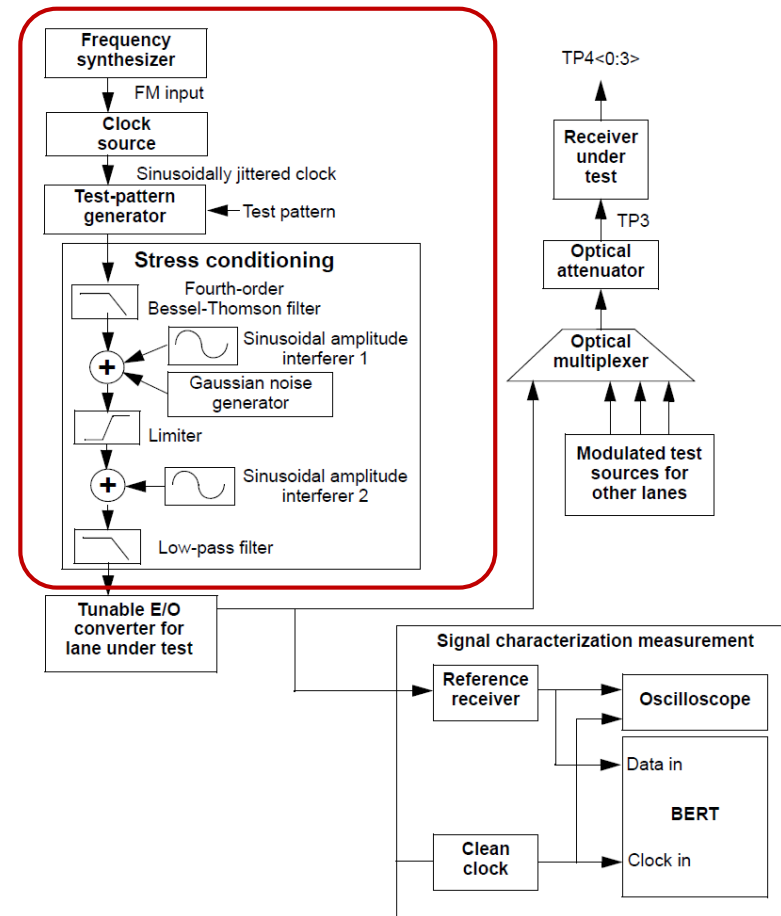


Figure 87-3—Stressed receiver conformance test block diagram

IEEE 802.3 Clause 87/88 Stressed RX Test Setup

Calibration of optical stressed test signal

Tunable E/O:

Tunable laser source to cover 1295-1310 nm

Reference Tx (MZ modulator)

Attenuator

Reference receiver:

Optical to electrical converter with BT4-filter response and reference frequency $f_t = 19.4$ GHz

Oscilloscope:

Use clean, un-jittered clock to verify stressed signal

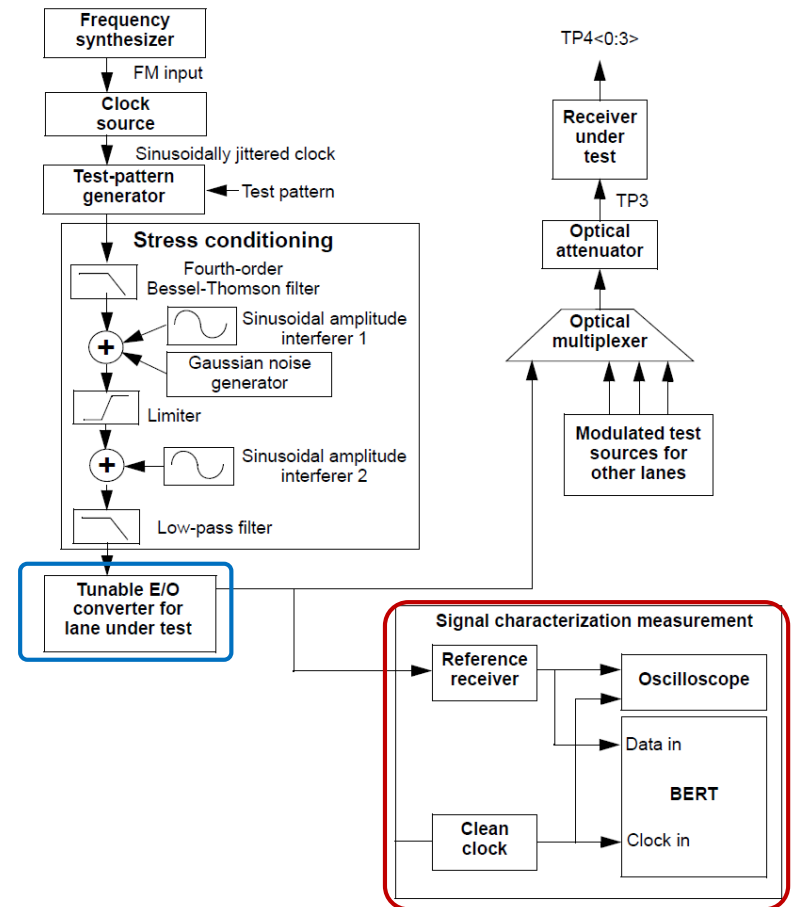
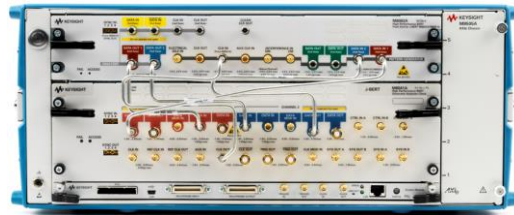


Figure 87-3—Stressed receiver conformance test block diagram

IEEE 802.3 Clause 87/88 Stressed Rx Test Setup

Generation of Electrical stressed test signal



Generation of Electrical amplitude interference



Generation of Optical stressed test signal



Stressed eye calibration

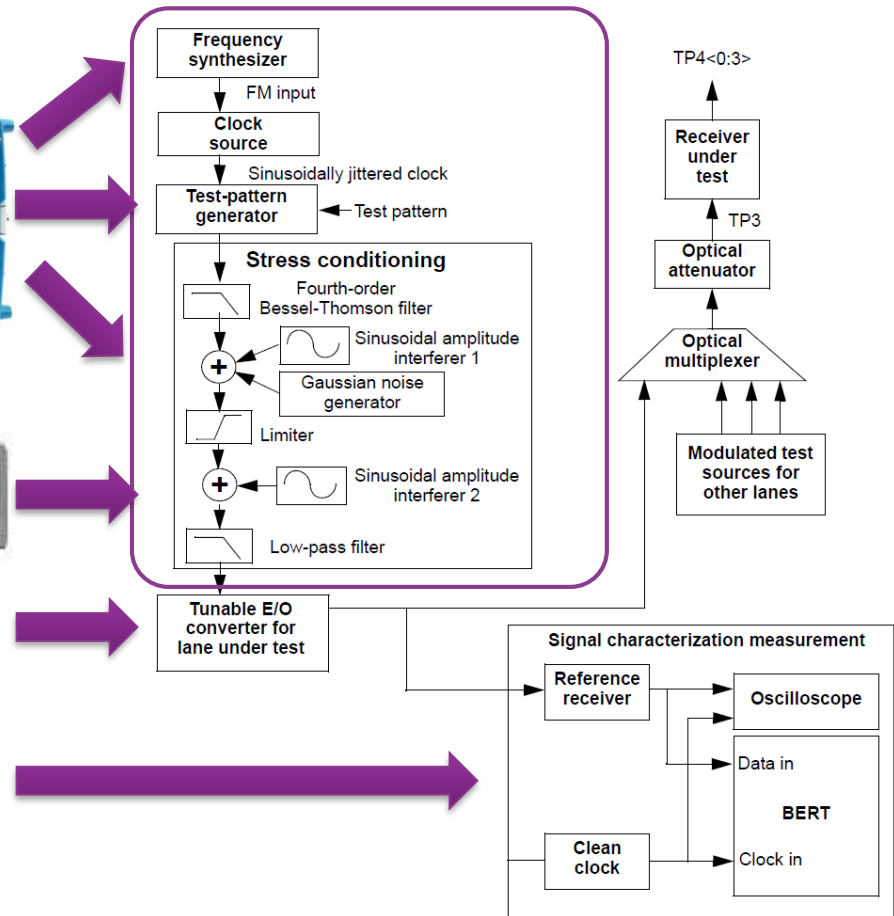
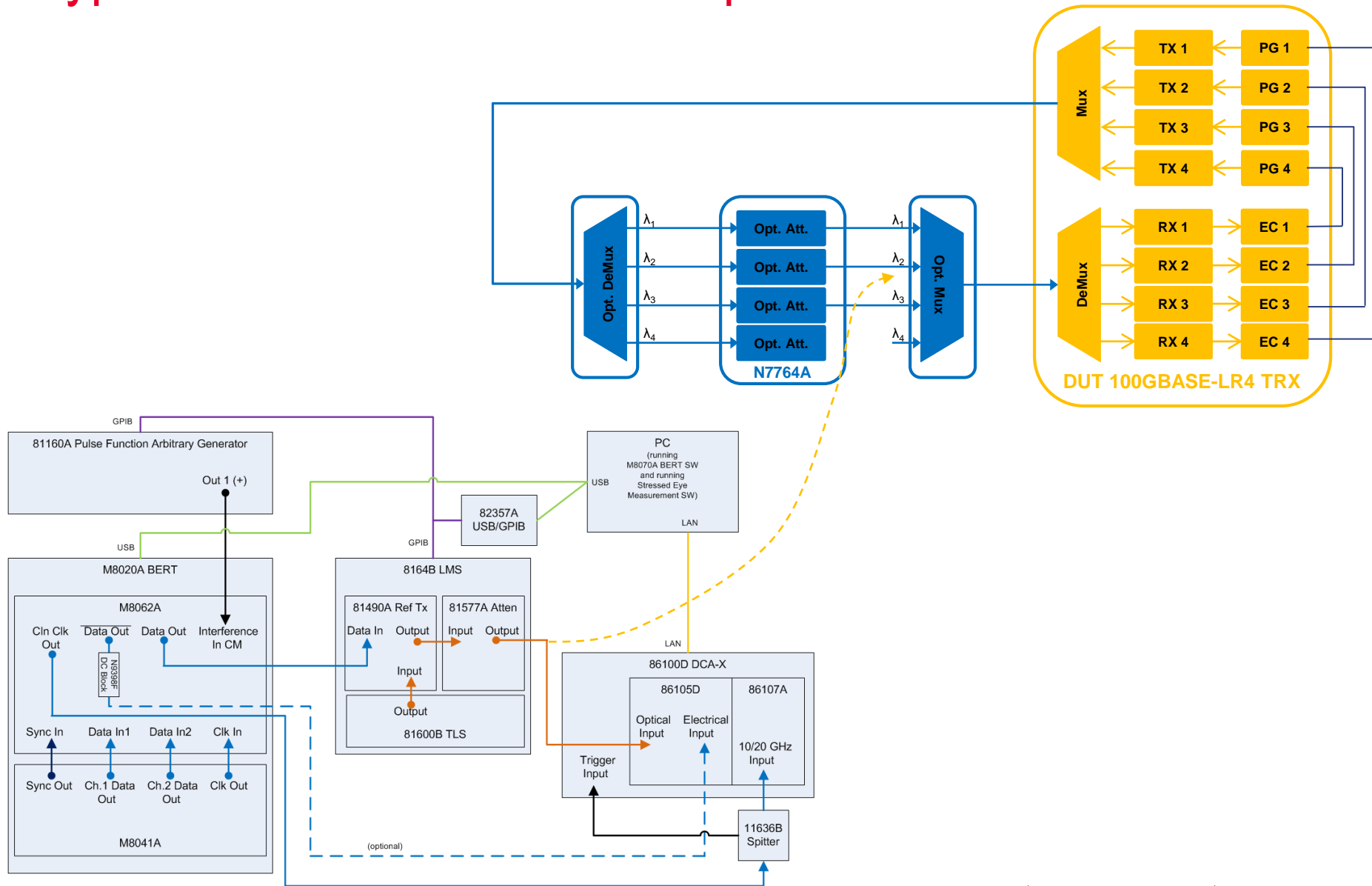


Figure 87–3—Stressed receiver conformance test block diagram

IEEE 802.3 – clause 87/88 proposed test set up

Typical Stressed Rx Test Setup – LR4 DUT test



Challenges with IEEE 802.3 Stressed Rx Test Setup

Typical issues faced with standard compliant test

- ❑ Test setup requires many different instruments operating seamlessly together.
- ❑ Standard details for characterization are referenced to various other parts within IEEE 802.3 making it difficult to cover all points.
- ❑ Optical stress parameters to be achieved are inter-dependent and therefore are not straight forward to set.
- ❑ LiNbO₃ based E/O converter is a device that drifts with temperature and operating conditions, requiring additional means to achieve repeatable and stable optical stressed eye.
- ❑ Knowledge about optical test is required to cope with polarization effects in E/O.

Agenda

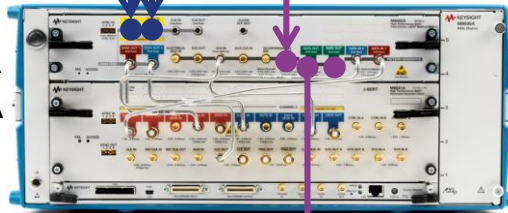
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Instruments for Optical Receiver Stress Test Solution

Signal Generator
81160, MXG or PSG
as SI source



J-BERT M8020A
with M8062A
32 Gb/s Front End



E/O 81490A-E05/09
Attenuator 81576/7A,
Tunable Laser 8160xx



DCA-X:
86100D, 86105D



BER < 10^{-12}
(full sampling with
recovered clock)

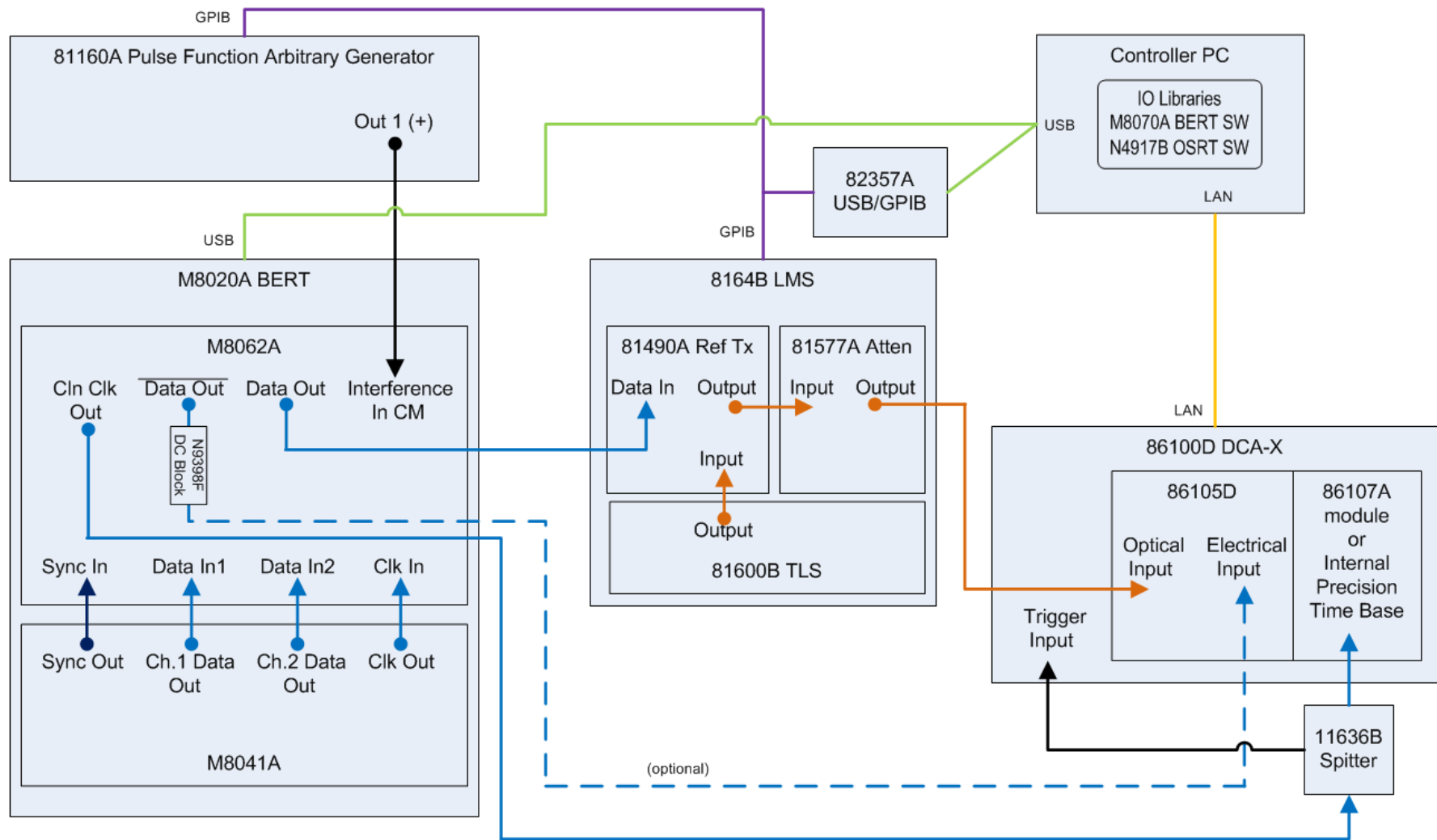
DUT: optical RX
(CFP2/CPAK)

1 of 4 lanes @
25.78 Gb/s

optical
stressed signal
to DUT (SM)

to DCA-X
for calibrating
signal and
checking setup

Typical Functional Block Diagram (with M8062A)



User interface

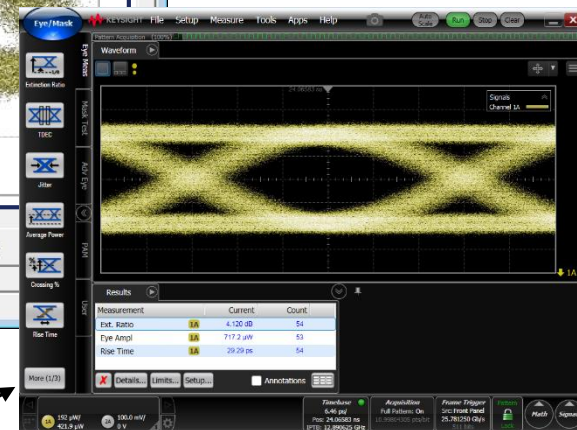
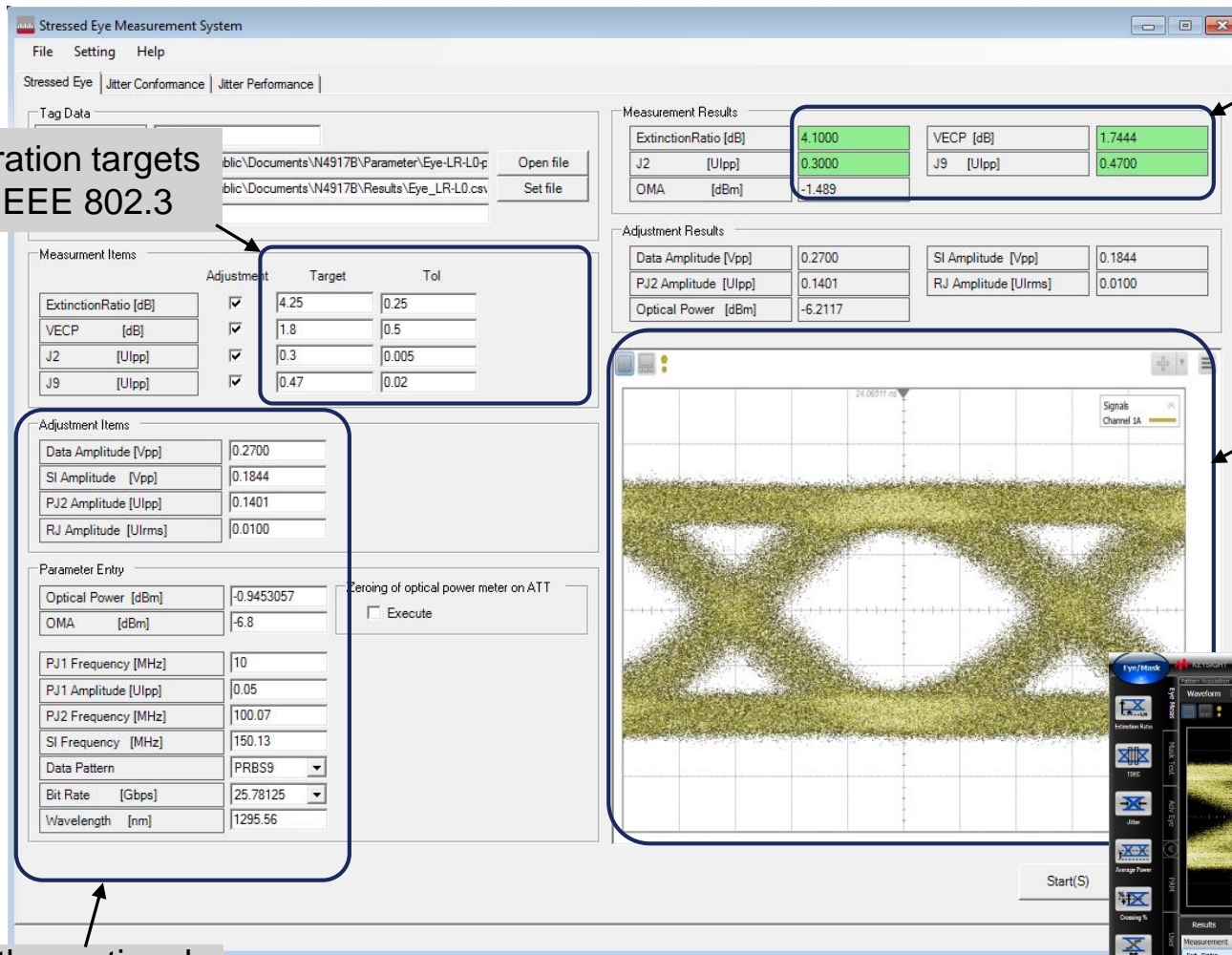
Calibration targets from IEEE 802.3

Results from calibration procedure

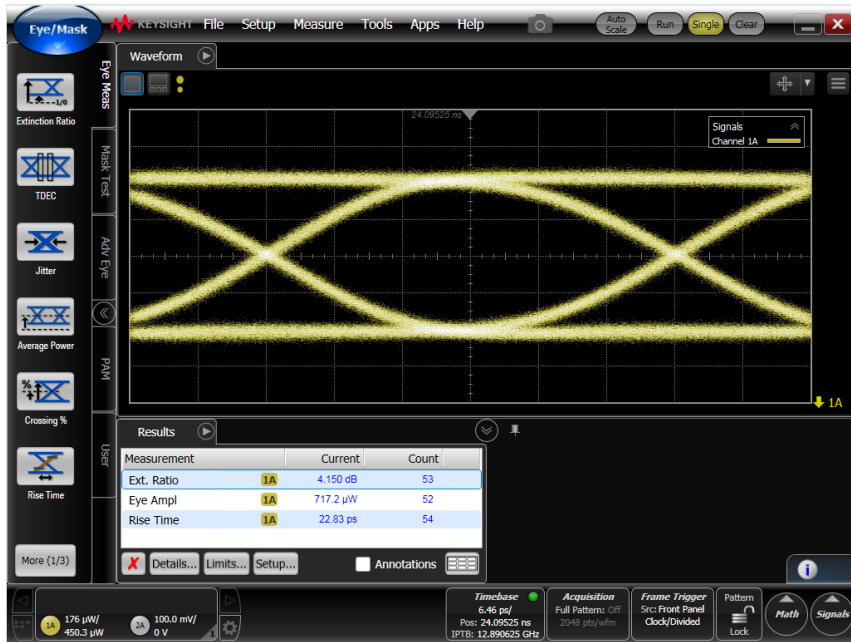
Optical stressed eye, loaded from DCA-X

Other optional parameters to modify

Optical stressed eye, on DCA-X



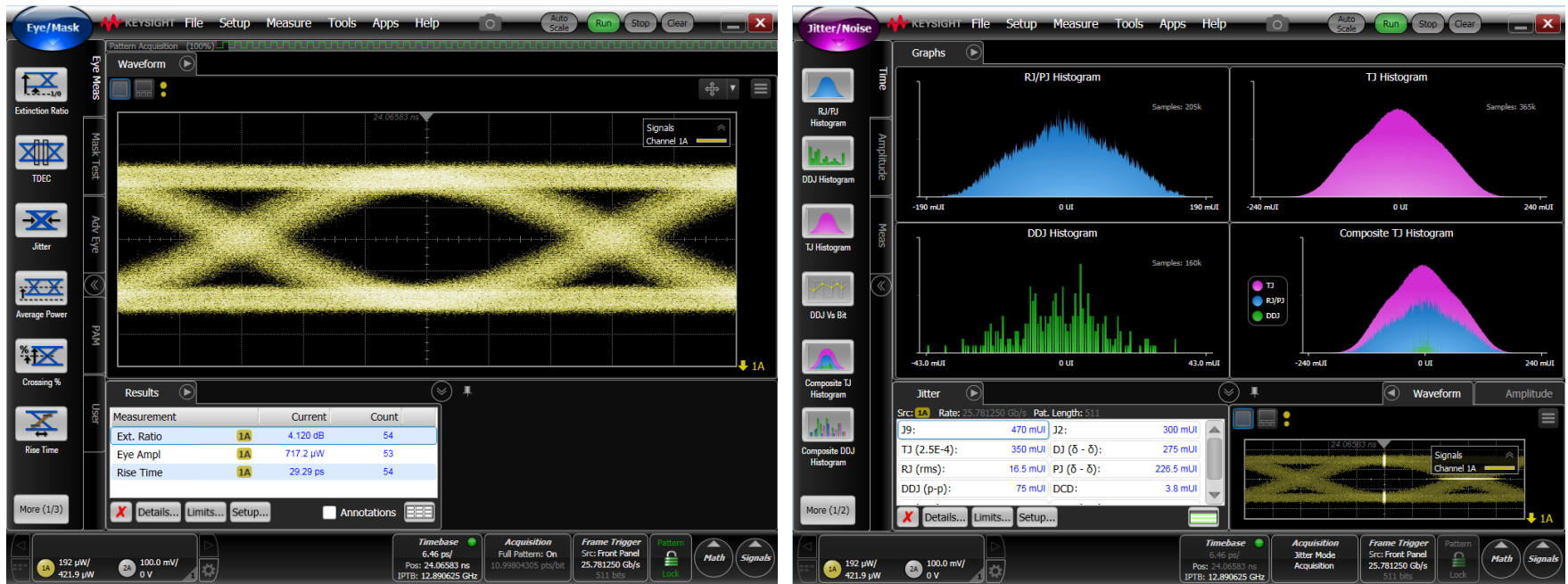
Unstressed Optical Eye Performance



Clean optical eye: ER = 4 dB, Bessel Thomson (BT-LPF) in DCA-X on

➤ Provides sufficient margin for standard compliant stress generation

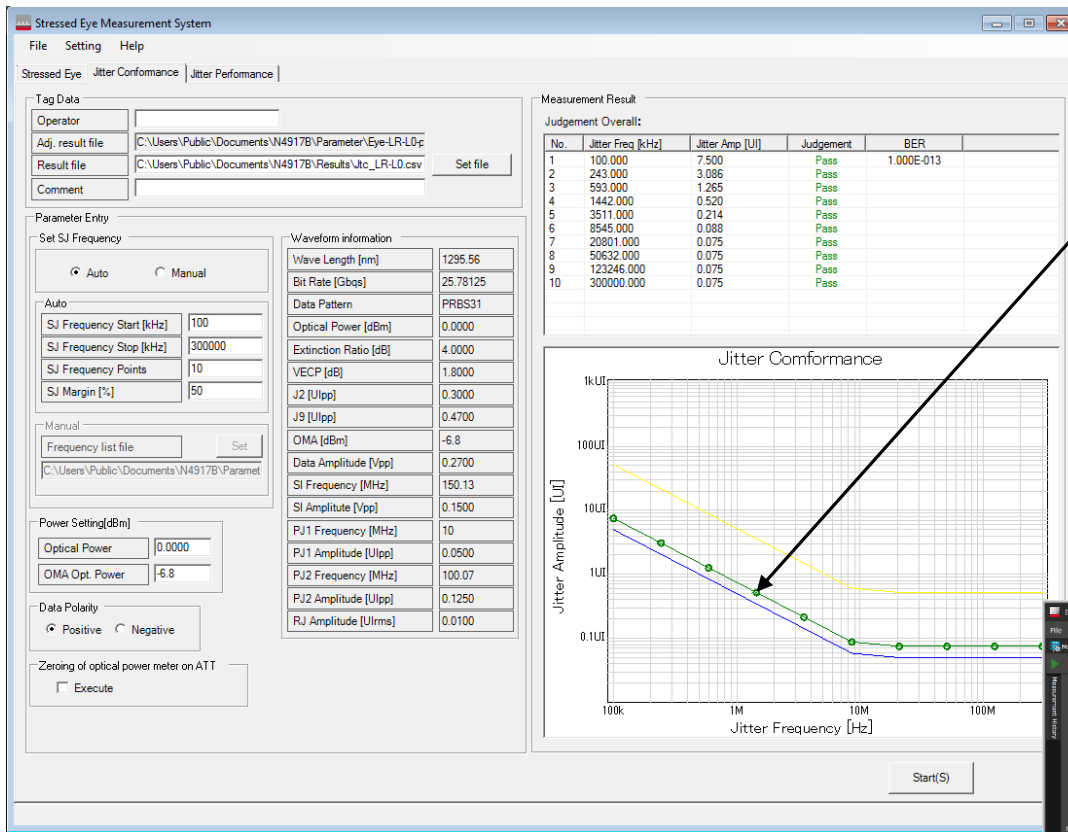
Stressed Optical Eye as required by IEEE802.3 cl. 88



Stressed optical eye parameters with

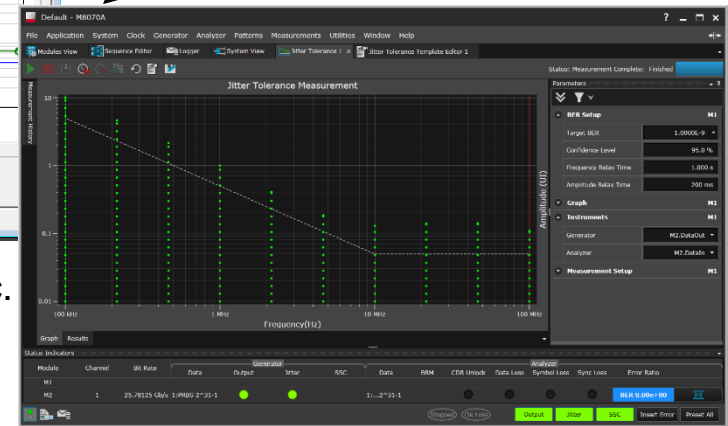
- VECP, ER, OMA, J2 and J9 targets achieved

Jitter Tolerance Test User Interface



Jitter tolerance margin testing – user specifies jitter and amplitudes and manually enters BER result.

Jitter tolerance margin testing – using M8070A with DUT control interface



Stressed eye tap for JTOL measurements are semi-automatic.

Alternatively use fully automated M8070A JTOL if:

- DUT can be looped back to M8020A analyzer, or
- DUT Control script used to talk to DUT error counters

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Supported and recommended equipment

BERT:

- M8020A with M8061A/N4877A or M8062A 32 Gb/s extensions



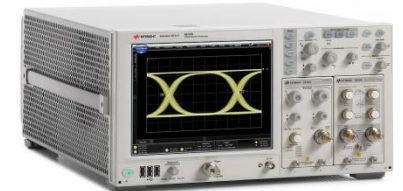
Optics:

- 8164B LMS mainframe
- 81602A-013, 81606A-113, 81608A-113, 81609A-113 TLS 86100B-132 (only recommended if already available at the customer)
- 81490A-E05 or E09 Ref Tx
- 81576/77A attenuator or external N77xx series attenuators



DCA:

- 86100D DCA-X with internal PTB or with 86107A PTB
- 86105D-281 Elect/Optical or 86115D-282 Optical modules



SI Source:

- 81160A Pulse Generator or EXG/MXG/PSG Signal Generator



Clock Source (optional)

- *EXG/MXG/PSG signal generator or external source*



The photograph shows a laboratory setup for testing an 81600B TLS device. The setup includes a laptop displaying a software interface, a Keysight M8041A microwave source, a Keysight 81600B TLS device, and a Keysight oscilloscope. The oscilloscope screen shows a waveform. A block diagram in the top right corner illustrates the connections between the devices, including Sync In/Out, Data In1/Out, Ch.1 Data Out, Ch.2 Data Out, Clk In/Out, and Trigger Input.